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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/995,423	11/27/2001	Wen-Chi Fang	U 013738-6	9763

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EXAMINER
NGUYEN, HAI L

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/995,423	FANG, WEN-CHI	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 & 09 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicants response received on 04/07/03 and 04/09/03 has been reviewed and considered with the following results:

The prior art rejections to claims 1-7 made in the previous Office Action are now withdrawn in view of Applicant's amendments. Applicant's amendments and arguments have been considered but are moot in view of a new action on the merits appears below.

As to the prior art rejections to claims 8-14, there is no response to the previous prior art rejections to those claims. Therefore, the prior art rejections to claims 8-14 are retained and repeated as set forth below.

Claim Objections

2. Claims 1 and 8 are objected to because of the following informalities: in line 1, "A universal clock" should be changed to --The universal clock--.

3. Claim 2 is objected to because of the following informalities: the claimed limitation "wherein the low frequency clock region is further connected to an oscillator" is redundant to the same limitation "an oscillator connected to the low frequency clock region" in claim 1. Therefore, claim 2 should be deleted.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ichinose et al. (US 5,696,950; previously cited) in view of Ishimi (US 6,157,226; previously cited).

With regard to claim 1, Ichinose et al. discloses in Figs.1-2 a clock generator circuit comprising a high frequency clock region (5, 6, 11, 12) for generating high frequency clocks (50 MHz, 66.6 MHz, 80 MHz; 24 MHz); and a low frequency clock region (8, 10, 14, 16) including a phase lock loop (14, 16) for generating low frequency clocks (1.84 MHz, 12 MHz); and an oscillator (204) connected to the low frequency clock region. Fig.1 of Ichinose et al. meets all the claimed limitations except for the limitation that the low frequency clock region is not including at least one delay lock loop (34) for increasing a number of the high frequency clocks of the high frequency clock region as recited in claim 1. Ishimi teaches in Figs.1-2 a low frequency clock (21) including a phase lock loop (40) for generating low frequency clocks; and at least one inherent delay lock loop (41) for inherently increasing a number of the high frequency clocks of the high frequency clock region. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to utilize that the low frequency clock circuit taught by Ishimi with the prior art (Fig.2 of Ichinose et al.) for the advantage of locking the phase accurately.

With regard to claims 2-5, the references also meet the claimed limitations in these claims.

With regard to claim 6, the above discussed the references meet all of the claimed limitations except for the limitation that the high frequency clock region and low frequency clock region are integrated into an IC. However, it is well known in the art to realize that the entire circuits can be integrated into an IC. Therefore, it would have been obvious to one of ordinary skill in the art to implement the prior art circuits by integrated into an IC for the advantage of reducing the surface area of the circuit.

With regard to claim 7, the above discussed the references meet all of the claimed limitations except for the limitation that the output pins of the high frequency clocks are set up as a push-pull, open-drain or differential output by a power-on setting pin as recited in claim 7. However, it would have been obvious to one of ordinary skill in the art to realize that the output pins of the high frequency clocks circuit of the prior art can be set up in many different ways as well, including set up as a push-pull, open-drain or differential output by a power-on setting pin, which is in each case optimally matched to its application.

With regard to claim 8, Ichinose et al. discloses in Fig.1 a clock generator circuit comprising a high frequency clock region (5-16) and a low frequency clock region(2). Fig.1 of Ichinose et al. meets all the claimed limitations except for the limitation that the low frequency clock region is not including a phase lock loop (33 in instant Fig.3) for generating low frequency clocks; and at least one delay lock loop (34) for increasing a number of the high frequency clocks of the high frequency clock region as recited in claim 1. Ishimi teaches in Figs.1-2 a low frequency clock (21) including a phase lock loop (40) for generating low frequency clocks; and

at least one inherent delay lock loop (41) for inherently increasing a number of the high frequency clocks of the high frequency clock region. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to utilize that the low frequency clock circuit taught by Ishimi with the prior art (Fig.2 of Ichinose et al.) for the advantage of locking the phase accurately.

Claims 9-14 are similarly rejected, note the above discussion with regard to claims 2-7.

Response to Arguments

6. Applicant's first argument is that "the patent teaches the obvious way of getting more clocks from more high frequency clock regions and not the claimed way of more clocks from only one high frequency clock region." is not persuasive because no such limitation as "more clocks from only one high frequency clock region" recited in the claim. Moreover, Ichinose et al. clearly meets that claimed limitation, since the high frequency clock region of Ichinose et al. also generates high frequency clocks as recited in claim 1, i.e., high frequency clocks 50 MHz, 66.6 MHz, 80 MHz have higher frequencies than the frequency clocks 1.84 MHz and 12MHz in low frequency clock region.

Applicant's second argument is that "The addition to the rejection of the Ishimi patent for disclosing a low frequency clock 21 including a phase lock loop 40 and at least one delay lock loop 41, at least because 41 is not a loop. In the Ishimi patent 41 is a "... phase locked circuit 41 (hereinafter it is also referred to as a phase locked section 41)" as at column 6, lines 31-33, and not a loop. As a result, it can only produece as many clocks as it has combinations digital delay lines, i.e., four in Fig. 2, and not the variables of the claimed delay lock loop" is not persuasive

because circuit 41 of Ishimi clearly has a functional of a delay lock loop circuit. For example, its output is a feedback signal (P1P through elements 22, 23, 37) for comparing to the input signal (INPUT CLOCK), then the delay line is adjusted base on comparison results by the phase comparator in order to maintain a constant delay of the output signal in relationship with the input signal. Therefore, circuit 41of Ishimi is a delay lock loop. Even though, Ishimi does not refer it as a delay lock loop.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 703-306-9178. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

HLN
June 10, 2003

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800